Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) An electronic device, comprising:

a first processor;

a second processor coupled to the first processor;

shared memory coupled to the first and second processors, wherein the shared memory includes the transmit memories of both the first and second processors; and

wherein the first processor is a master processor that manages the shared memory and ~~exclusively~~ ~~dynamically~~ allocates a message buffer to the second processor based on a specific request from the second processor to send a message to the first processor, and wherein the first processor sends a message buffer pointer to the second processor that directs the second processor to the message buffer.

2. (original) An electronic device as defined in claim 1, wherein the first processor sends the message buffer pointer to the second processor in response to receiving an empty buffer request from the second processor.

3. (original) An electronic device as defined in claim 2, wherein after receiving the message buffer pointer the second processor fills the message buffer with the message.

4. (original) An electronic device as defined in claim 3, wherein after filling up the message buffer with the message, the second processor passes the message buffer pointer to the first processor.

5. (original) An electronic device as defined in claim 4, wherein the first processor reads the message from the message buffer after receiving the message buffer pointer.

6. (original) An electronic device as defined in claim 5, wherein after reading the message, the first processor releases the message buffer.

7. (original) An electronic device as defined in claim 1, wherein a plurality of buffers assigned to the second processor are located in the shared memory.

8. (original) An electronic device as defined in claim 7, wherein the plurality of buffers assigned to the second processor are used by the second processor without having to request them from the first processor.

9. (original) An electronic device as defined in claim 8, wherein when the second processor needs to send a message to the first processor it loads a starting address of the message in one of the plurality of buffers assigned to the second processor.

10. (original) An electronic device as defined in claim 1, wherein the electronic device comprises a radio communication device.

---

11. (currently amended) A method for providing interprocessor communication between first and second processors using a shared memory that includes the transmit memories of the first and second processors, the first processor being a master processor assigned to manage the shared memory ~~by at least exclusively allocating the shared memory~~, the method comprising the steps of:

(a) sending a request from the second processor requesting an empty message buffer from the shared memory when the second processor needs to send a message to the first processor;

(b) sending a message buffer pointer from the first processor to the second processor in response to the request sent in step (a);

(c) using the message buffer pointer by the second processor to locate the empty message buffer in the shared memory where the message is going to be loaded; and

(d) loading the empty message buffer with the message.

12. (original) A method as defined in 11, further comprising the step of:

(e) sending the message buffer pointer back to the first processor.

13. (original) A method as defined in claim 12, wherein in response to step (e) the first processor performs the step of:

(f) reading the message.

14. (original) A method as defined in claim 13, further comprising the step of:

~~(g) releasing the empty message buffer once step (f) has been performed.~~

15. (currently amended) A method for providing interprocessor communication between first and second processors using a shared memory that includes the transmit memories of the first and second processors, the first processor being a master processor assigned to manage the shared memory, the method comprising the steps of:

at the first processor:

(a) ~~exclusively dynamically~~ allocating a memory buffer from the shared memory for use in loading a message to be sent to the second processor in response to a specific request from the second processor;

(b) loading the message in the memory buffer;

(c) sending a message buffer pointer to the second processor; and

at the second processor:

(d) using the message buffer pointer to locate the message in the shared memory.

16. (original) A method as defined in claim 15, further comprising the step of:

at the second processor:

(e) reading the message; and

(f) sending the message buffer pointer back to the first processor.

17. (original) A method as defined in claim 16, wherein the first processor upon receiving the message buffer pointer sent in step (f), releases the allocated memory buffer so it can be used for a future message.

18. (original) A method as defined in 15, wherein step (c) is performed by the first processor sending the starting address of the allocated memory buffer to a memory located in the second processor.

19. (original) A method as defined in claim 18, wherein the first processor sends an interrupt to the second processor once it has loaded the starting address of the allocated memory buffer in the memory located in the second processor.